contactless transmission of data containing information about a test result.

Claim 24(new). The test configuration according to claim 23, including a receiver disposed separate from said semiconductor chip, said functional unit having an output terminal through which the data to be transmitted can be transmitted by capacitive coupling to said receiver.

C1 cont.

Claim 25(new). The test configuration according to claim 23, wherein said semiconductor chip has a detector selected from the group consisting of voltage detectors and current detectors, said detector is connected to said energy source and to said functional unit for initiating a data transmission by said functional unit due to a detected characteristic voltage sequence or current sequence.

Claim 26(new). The test configuration according to claim 20, wherein said semiconductor chip has a terminal and a nonvolatile memory unit for storing data containing information about a test result, said nonvolatile memory unit being connected to said terminal through which the data of said nonvolatile memory unit can be tapped off to a point outside said semiconductor chip.

Claim 27(new). The test configuration according to claim 20, wherein one of said semiconductor chips is decoupled from respective others of said semiconductor chips with regard to said energy supply during a functional test.

Claim 28(new). The test configuration according to claim 20, wherein all of said semiconductor chips to be tested are connected to said energy source being a common energy source, each of said semiconductor chips has a current limiter circuit for electrically isolating a respective semiconductor chip from said common energy source in an event of a limit value of an operating current being exceeded.

Claim 29(new). The test configuration according to claim 20, wherein each of said semiconductor chips has an integrated memory containing memory cells to be subjected to a functional test, and said self-test unit generates test information and carries out a functional test of said memory cells.

Claim 30(new). The test configuration according to claim 29, wherein said integrated memory has normal memory cells and redundant memory cells for replacing said normal memory cells, and said self-test unit is configured for checking a functionality of said normal memory cells, for analyzing which of said normal memory cells are to be replaced by which of

said redundant memory cells, and for activating said redundant memory cells in accordance with a result of the analysis.

Claim 31(new). The test configuration according to claim 30, wherein said integrated memory has electrically programmable memory units for activating said redundant memory cells, in which a repair result determined by said self-test unit can be programmed.